STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES

Abstract

Structures and methods involving at least a pair of gate oxides having different thicknesses, one suitable for use in a logic device and one suitable for use in a memory device, have been shown. The method provided by the present invention affords a technique for ultra thin dual gate oxides having different thicknesses using a low temperature process in which no etching steps are required. The method includes forming a pair of gate oxides to a first thickness, which in one embodiment, includes a thickness of less than 5 nanometers. In one embodiment, forming the pair of gate oxides includes using a low-temperature oxidation method. A thin dielectric layer is then formed on one of the pair of gate oxides which is to remain as a thin gate oxide region for a transistor for use in a logic device. The thin dielectric layer exhibits a high resistance to oxidation at high temperatures. In one embodiment, the thin dielectric layer includes a thin dielectric layer of silicon nitride (Si_3N_4) formed using jet vapor deposition (JVD). The other of the pair of gate oxides is then formed to a second thickness to serve as a thick gate oxide region for a transistor for use in a memory device. Another embodiment of the present invention includes the structure of a logic device and a memory device formed on a single substrate as well as systems formed according to the method described above. In one embodiment, a dielectric layer of the transistor for use in the logic device has a thickness of less than 7 nanometers and a dielectric layer in the transistor for use in the memory device has a thickness of less than 12 nanometers.